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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/932,334	08/17/2001	Iain Robertson	TI-26018	4190

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EXAMINER

MARTINEZ, DAVID E

ART UNIT PAPER NUMBER

2182

DATE MAILED: 03/29/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

**Office Action Summary**

Application No.

09/932,334

Applicant(s)

ROBERTSON, IAIN

Examiner

David E Martinez

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 09 February 2004.
- 2a) ☐ This action is FINAL. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 1-11 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☒ Claim(s) 8-11 is/are allowed.
- 6) ☒ Claim(s) 1-7 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

  
FRITZ FLEMING  
PRIMARY EXAMINER  
GROUP 2100

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some \* c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
  2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- \* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)  
Paper No(s)/Mail Date \_\_\_\_\_
- 4) ☐ Interview Summary (PTO-413)  
Paper No(s)/Mail Date. \_\_\_\_\_
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: \_\_\_\_\_

## DETAILED ACTION

### *Claim Rejections - 35 USC § 103*

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

1. Claims 1-7 are rejected under 35 U.S.C. 103(a) as being unpatentable over US Patent No. 6,401,149 to Dennin et al. (Dennin) in view of US Patent No. 5,450,546 to Krakirian.

2. With regards to claim 1 and 5, Dennin teaches a data transfer apparatus transferring data from a data source to a data destination comprising:

a first-in-first-out buffer memory [fig 4, element 302, column 7 lines 35-41] having an input connected to the data source, an output connected to said data destination [figs 3,4 column 6 line 46 to column 7, line 12] and a predetermined number of data entries [fig 4, element 402, column 7, lines 35-41];

a remote queue counter [fig 4, element 414] storing a remote count indicative of a number of data entries within said first-in-first-out buffer memory currently storing data [column 8, lines 57-61], said remote queue counter connected to said data source for incrementing said remote count upon allocation of data at said data source to be stored in said first-in-first-out buffer memory [fig 4, element 130 bus to data source], connected to said data destination for decrementing said remote count [fig 4, element 414, is part of the FIFO memory element 302, that is connected to the data destination, figs 3,4 column 6 line 46 to column 7, line 12] and generating a decrement confirmation signal upon transfer of data out of said first-in-first-out buffer memory to said data destination; and

Dennin teaches all of the above limitations except for a master queue counter storing a master count indicative of a number of data entries available for data storage within said first-in-first-out buffer memory, said master queue counter connected to the data source to decrement said master count upon allocation of data at said data source to be stored in said first-in-first-out buffer memory; wherein said master queue counter is further connected to said remote queue counter for incrementing said master count upon receipt of said decrement confirmation signal.

However, Krakirian teaches a master queue counter storing a master count indicative of a number of data entries available for data storage within a first-in-first-out buffer memory, said master queue counter connected to the data source to decrement said master count upon allocation of data at said data source to be stored in said first-in-first-out buffer memory; wherein a master queue counter is further connected to a remote queue counter for incrementing a master count upon receipt of a decrement confirmation signal ['second counter' column 4 lines 19-36 and line 62 to column 5 line 16, 'block counter' column 7 lines 30-61 and column 8 lines 29-39]. Krakirian discloses by using counters to monitor how full and empty a fifo buffer memory is, benefit a system by minimizing processor involment thus improving performance.

It would have been obvious to one of ordinary skill in the art at the time of the invention to combine the teachings of both Dennin and Krakirian to provide a master queue counter storing a master count indicative of a number of data entries available for data storage within said first-in-first-out buffer memory, said master queue counter connected to the data source to decrement said master count upon allocation of data at said data source to be stored in said first-in-first-out buffer memory; wherein said master queue counter is further connected to said remote queue counter for incrementing said master count upon receipt of said decrement

confirmation signal in order to use counters to monitor how full and empty a fifo buffer memory is to benefit a system by minimizing processor involvement thus improving performance.

3. With regards to claims 2 and 6, Dennin teaches the data transfer apparatus of claim 1, wherein:

said remote queue counter is initialized at zero [column 16 lines 1-4 initialized to a default value, column 10 lines 6-8].

Dennis teaches the above limitation except for said master queue counter is initialized to said predetermined number of data entries of said first-in-first out buffer memory;

However, Krakirian teaches a master queue counter used to keep track of how empty a fifo buffer memory is, and is initialized to a predetermined number of data entries of [column 4 lines 19-36, column 7 lines 30-61] for being able to keep track of the number of empty data entries in the fifo buffer memory. Krakirian teaches the initialization of the master queue counter being arbitrarily chosen as the maximum or the minimum value of the fifo buffer memory. He discloses the example of initializing the master queue counter at the maximum number then decrementing it as the fifo buffer memory gets filled.

It would have been obvious to one of ordinary skill in the art at the time of the invention to combine the teachings of both Dennin and Krakirian to have master queue counter initialized to the predetermined number of data entries of the first-in-first out buffer memory to keep be able to have the number of empty data entries for the same reasons as set forth above in claim 1.

4. With regards to claims 3, and further regards to claim 5, Dennin teaches the data transfer apparatus of claim 1, wherein:

said data destination reads said first-in-first-out buffer memory only if said remote queue counter is non-zero [column 10 lines 13-23].

Dennin fails to teach a data source may allocate data to a first-in first-out buffer memory only if a master queue counter indicates a non-zero number of data entries available for data storage within said first-in-first-out buffer memory. However, Krakirian teaches a data source may allocate data to a fifo buffer memory only if a master queue counter indicates a non-zero number of data entries available for data storage within said fifo buffer memory [column 4 lines 27-42] for the benefit of preventing buffer overflow.

It would have been obvious to one of ordinary skill in the art at the time of the invention to combine the teachings of both Dennin and Krakirian to have a data source allocate data to a first-in first-out buffer memory only if a master queue counter indicates a non-zero number of data entries available for data storage within said first-in-first-out buffer memory for the benefit of preventing buffer overflow.

5. With regards to claims 4 and 7, Dennin teaches the data transfer apparatus of claim 1, wherein:

said data source may selectively annul allocation of data of said data source to be stored in said first-in-first-out buffer memory [column 8 lines 32-34, column 11, lines 21-25, column 12, table 2, lines 20-25, the 'Stop FIFO' Command stops any active commands which as Table 2 shows, could be 'Read from Buffer Memory' or 'Write to Buffer Memory' thus annulling allocation of data of said data source to be stored in said fifo buffer memory]

Dennin teaches the above limitations except for said data source generating an annul increment signal upon annulling data; and

said master queue counter is further connected to said data source to increment said master count upon receipt of said annul increment signal.

However, Krakirian teaches a master queue counter is connected to a data source that increments and decrements upon the receipt of a confirmation signal for monitoring how full and

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empty a fifo buffer memory is, to benefit a system by minimizing processor involvement thus improving performance.

It would have been obvious to one of ordinary skill in the art at the time of the invention to combine the teachings of both Dennin and Krakirian to have the data source generate an annul increment signal upon annulling data, and to have said master queue counter connected to said data source to increment said master count upon receipt of said annul increment signal to be able to determine how full and how empty a fifo buffer memory is, to improve performance by minimizing processor involment by letting the counter keep track of data flow.

#### ***Allowable Subject Matter***

6. Claim 8-11 are allowed over the prior art.

The following is a statement of reasons for the indication of allowable subject matter:

With regards to claims 8-11, the prior art alone or in combination do not teach the various pipelining stages when events occur for the claimed invention.

#### ***Response to Arguments***

7. Applicant's arguments with respect to claims 1-7 have been considered but are moot in view of the new ground(s) of rejection.

#### ***Conclusion***

Any inquiry concerning this communication or earlier communications from the examiner should be directed to David E Martinez whose telephone number is (703) 305-4890. The examiner can normally be reached on 8:30-5:00 M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jeffrey A Gaffin can be reached on (703) 308-3301. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

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Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

DEM

  
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